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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,469	01/06/2004	Jeong-won Lee	Q77017	2348

23373 7590 09/08/2005

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/751,469	LEE ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amendment filed on 07/05/05. Claims 1 – 6 remain in this application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Response to Arguments

3. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipate by Ueunten U.S. Patent No. 5,412,309.

Regarding claim 1, Fig. 8 of Ueunten discloses a amplifier circuit, comprising: an input circuit part (M1, M2) for outputting a differential current (output current of M1, M2),) proportional to differentiations of input voltages (199, 198); a bias circuit part (Q4 – Q7) for mirroring the differential current, inverting the differential current, and producing an inverted differential current (I1, I3); and an output circuit part (202, 203) for adjusting each magnitude of the differential current (I1, I3) based on a predetermined ratio size of MOS transistors ([205-3, 205-2]; [206-1, 206-2]) of the output circuit part (202, 203), to output an adjusted differential current (Iout = 601*I1) and an adjusted inverted differential current (Iout = 601*I3), adding the adjusted differential current and the adjusted inverted differential current (summing at the Node of 222 Vout), and producing an output current in a push-pull form (the current output at the summing node 222 is representing the current output in a push-pull form of 202 and 203 respectively).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueunten as applied to claim 1 above, in view of Fenk U.S. Patent No.4,369,410.

Regarding claim 2, Fig. 8 of Ueunten as applied to claim 1 above does not discloses wherein the input circuit part includes: a second differentiation circuit for being inputted with the reference voltage and a second input voltage of the input voltages.

Fig. 1 of Fenk discloses a differential amplifier circuit for generating an output different output current (15) and inverted different output current (16) having a first differentiation circuit (1, 2)) for being inputted with a reference voltage (node at the gates of 2 and 3) and a first input voltage (13) of the input voltages (13, 14), and outputting a first differential current (15); a second differentiation circuit (3, 4)) for being inputted with the reference voltage (node at the gates of 2 and 3) and a second input voltage (14) at of the input voltages (13, 14), and outputting a second differential current (16).

Ueunten et al. and Fenk are common subject matter for differential amplifier circuit for generating first and second output current. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the differential input circuit taught by Fenk into the input differential circuit of Ueunten et al. for the purpose of providing first and second pair amplifier input circuit with a common reference voltage.

Regarding claim 5, Fig. 8 of Ueunten et al. modified by Fen et al. further discloses wherein the bias circuit part mirrors (Q4, Q5) the first differential current and produces a first inverted differential current (I1) wherein the first differential current is

inverted, and mirrors (Q6, Q7) the second differential current and produces a second inverted differential current (I3) wherein the second differential current is inverted.

Regarding claim 6, wherein the output circuit part includes (202, 203) a first output part (202) for adjusting each magnitude of the first differential current and the second inverted differential current based on the predetermined size ratio of a first MOS transistor (205-1, 205-2, 205-3) and adding (Node at 222) the adjusted magnitudes of the first differential current and the second inverted differential current (I1, I3), thereby outputting a first output current (601*I1); and a second output part (203) for adjusting each magnitude of the second differential current and the first inverted differential current (I1, I3) based on the predetermined size ratio of a second MOS transistor (206 – 1, 206 - 2) and adding (Node at 222) the adjusted magnitudes of the second differential current and the first inverting differential current (I1, I3) , thereby outputting a second output current (I0ut = 601*I3), and the output current (Iout at node Vout 222) being produced by adding (Node at Vout 222) the first and second output currents (current outputs of 202, 203).

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueunten in view of Fenk as applied to claim 2 above, and further view of Mullins et al. U.S. Patent No. 5, 592,124.

Regarding claim 3,Ueunten in view of Fenk as applied to claim 2 above disclosed every aspect of applicant claimed invention except for a capacitor in each differential amplifier circuit.

Fig. 1 of Mullins discloses a differential amplifier circuit (10, 11) having capacitor (16) coupled between the input gate 10 and Input signal terminal 3.

Ueunten/Fenk and Mullins et al. are common subject matter for differential input amplifier circuit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the capacitor taught (16) taught by Mullins et al. into the Ueunten/Fenk for the purpose of providing good frequency response for the circuit and improve input referred noise characteristic of the circuit (Mullins et al. Col 6. lines 54 – 58).

Regarding claim 4, Ueunten/Fenk combined with Mullins et al. as applied to claim 3 above, further discloses wherein the fully differential operational amplifier has input terminals formed with NPN bipolar transistors in a left to right symmetry (Fig. 1 of Fenk).

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

9/4/05

Linh Van Nguyen

Art Unit 2819